

Notice of References Cited	Application/Control No. 10/015,180	Applicant(s)/Patent Under Reexamination JAIN ET AL.	
	Examiner Thomas H. Stevens	Art Unit 2123	Page 1 of 1

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	C	US-5,379,231	01-1995	Pillage et al.	703/14
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NON-PATENT DOCUMENTS

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*	U	Pandey et al., "VHDL Semantics and Validateing Transformations" IEEE July 1999, vol 18., no. 7. pg., 936-955
*	V	Gregory-B., "Avoiding HDL Synthesis Pitfalls" Synopsis Inc. 1994, Electronic Product Design vol.15, no. 2, pg. 23-24
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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.